Amendments to the Claims:

Please amend the claims as shown below. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-14. (Canceled)

15. (Currently amended) A method for fabricating a circuit component, comprising:

providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump; ~~and~~

after said providing said exposed metallization structure, performing a sputter etching process with an argon gas; and[[.]]

after said performing said sputter etching process, contacting said metal bump with a testing probe.

16-26. (Canceled)

27. (Currently amended) A method for fabricating a circuit component, comprising:

providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between

said first region and said sidewall, and a passivation layer over said semiconductor wafer and on said second region, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump; ~~and~~

after said providing said exposed metallization structure, performing an ion milling process with an argon gas; and[[.]]

after said performing said ion milling process, contacting said metal bump with a testing probe.

28-34. (Canceled)

35. (Canceled)

36. (Canceled)

37. (Currently amended) A method for fabricating a circuit component, comprising:

providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure directly on said passivation layer, on said first region and over said semiconductor wafer, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump; ~~and~~

after said providing said exposed metallization structure, performing an ion milling process with an inert gas; and[[.]]

after said performing said ion milling process, contacting said metal bump with a testing probe.

38. (Previously Presented) The method of claim 37, wherein said inert gas comprises an argon gas.

39. (Previously presented) The method of claim 37, wherein said inert gas comprises a helium gas.

40. (Canceled)

41. (Canceled)